ABSTRACT

1   A method and system for generating a data clock having
2   edge coincidence with an aggregate PN code is provided.
3   The method includes providing an aggregate PN code
4   generator having an epoch output for resetting a data
5   clock generator when the aggregate PN code generator
6   generates an epoch signal. Between resets the data clock
7   generator divides a PN master clock signal with a divisor
8   derived from the prime factor(s) of one or two of PN
9   codes used to form the aggregate PN code.